**EE307 Digital Electronics and Integrated Circuits**

**Class Final**, **March 17, 2014**

**NAME:**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

No calculators. Only use documents on the PolyLearn page that I prepared for this exam.

No cheating or I reserve the right to fail you in this class and report you.

Show work where asked (or no credit!).

Rules:

**I will not talk about this exam with anyone that hasn’t taken it yet.**

**Signature:**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

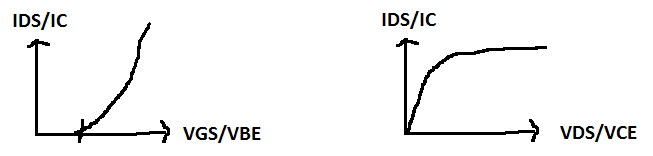
|  |  |  |
| --- | --- | --- |
| Question | Pts | Score |
| 1a-b | 6 |  |
| 2a-c | 13 |  |
| 3a-c | 9 |  |
| 4a-k | 22 |  |
| 5 | 6 |  |
| 6 | 5 |  |
| 7a-b | 10 |  |
| 8a-b | 8 |  |
| 9a-b | 10 |  |
| 10a-b | 7 |  |
| Total | 106 |  |

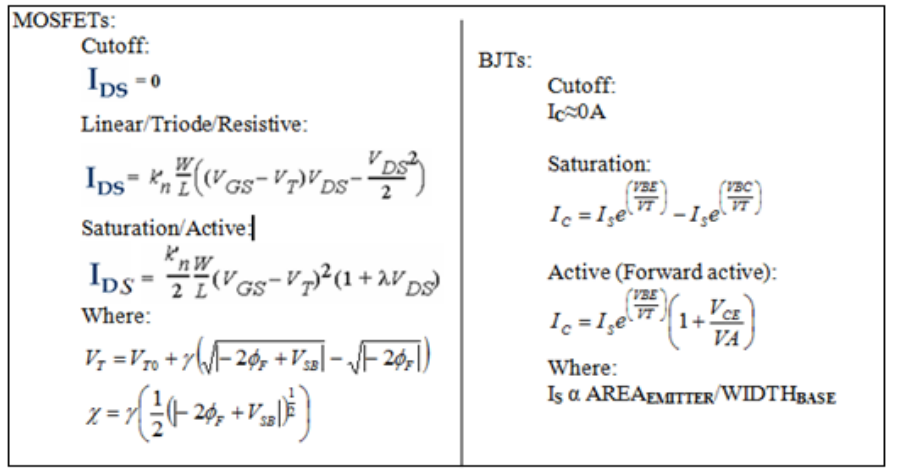
|  |  |
| --- | --- |
| Powers of Euler’s #, e | |
| Power | Value |
| 1 | 2.718282 |
| 2 | 7.389056 |
| 3 | 20.08554 |
| 4 | 54.59815 |
| 5 | 148.4132 |
| 6 | 403.4288 |
| 7 | 1096.633 |

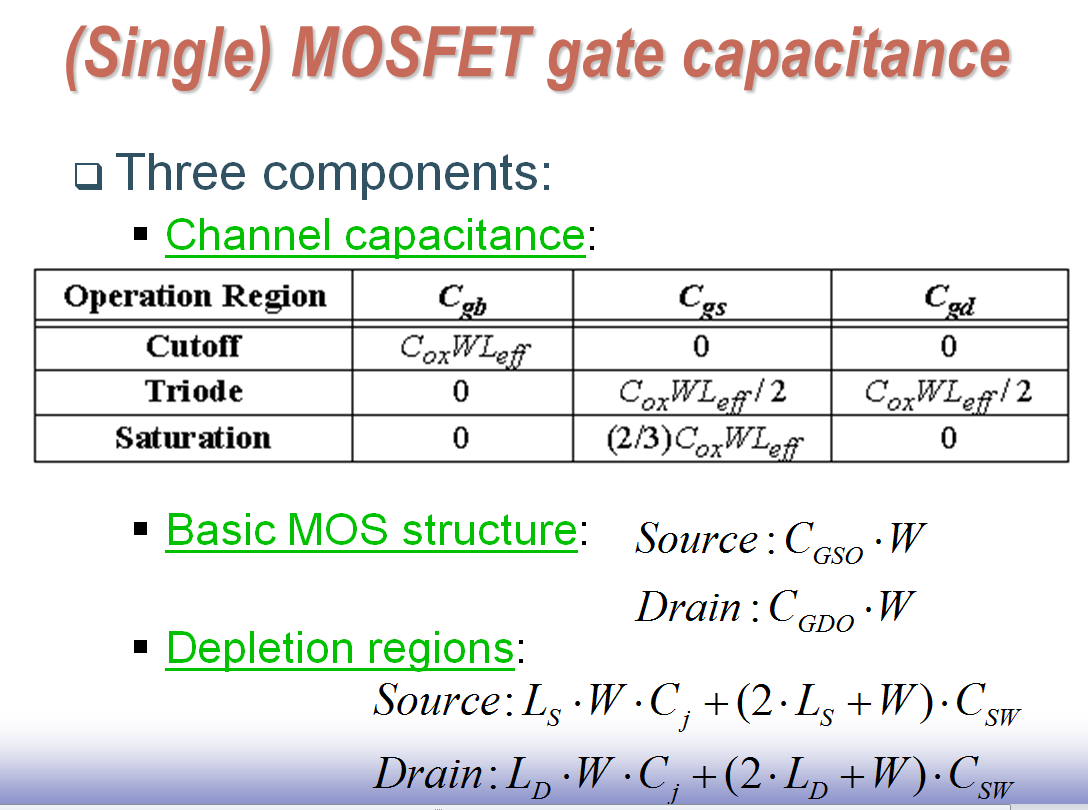
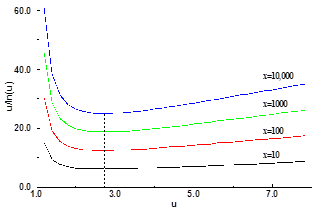
Inverter sizing: 

Delay: 

Power: 





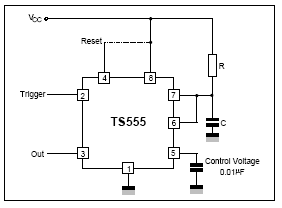
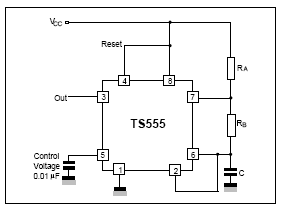
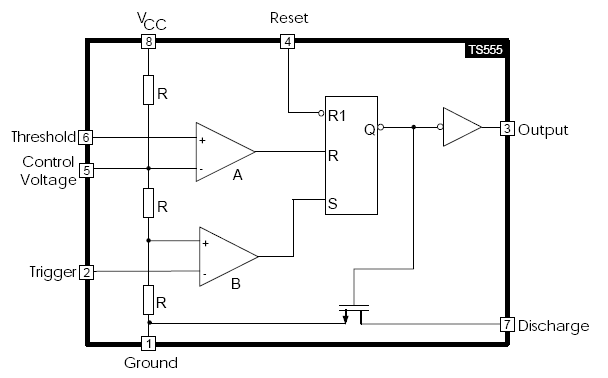


‘***f***’ values and delay. Minimum at ‘e’.

Definition: VTC or transfer characteristics: Vout on Y-axis, Vin on X-axis. More generally: Input on X-axis, output on Y-axis.

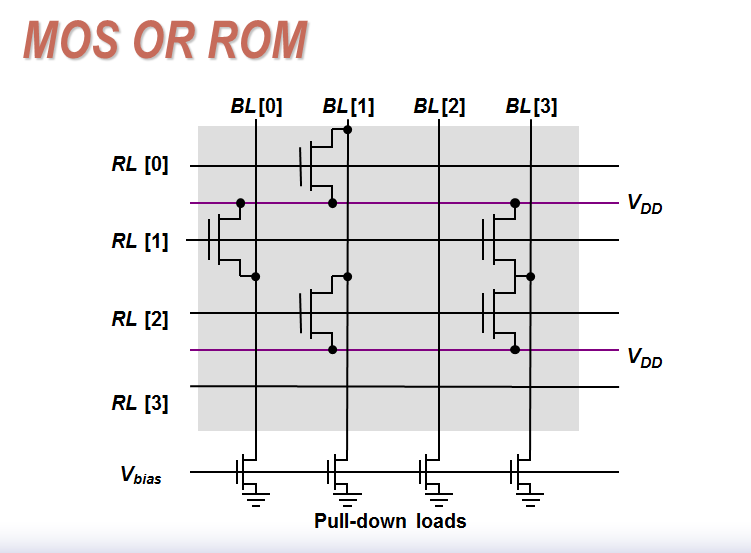
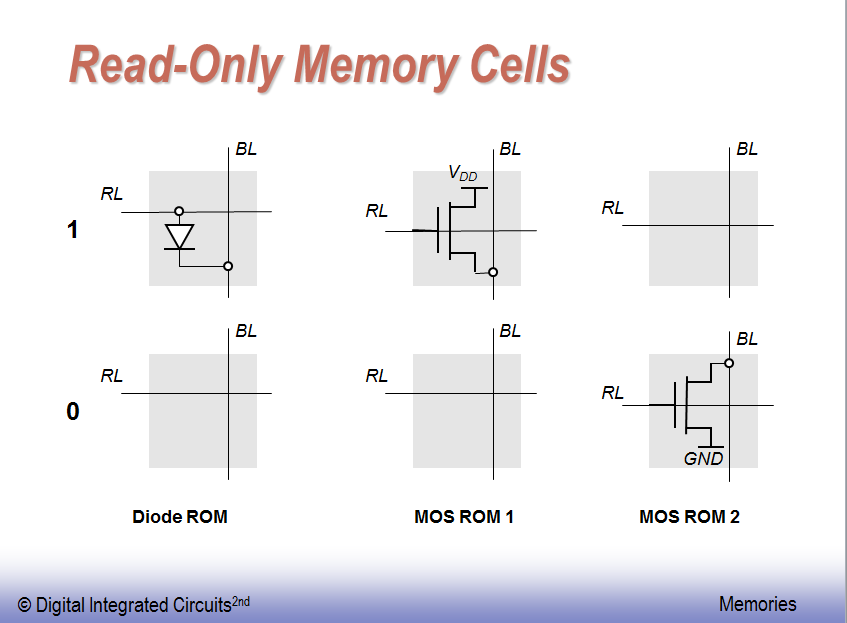
Definition of “Forward active” for BJTs includes both VCEsat and PN junction requirements.

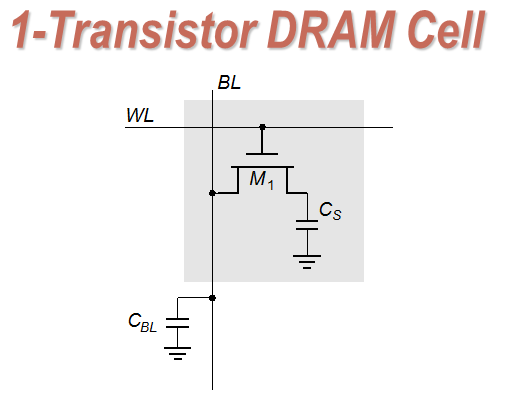
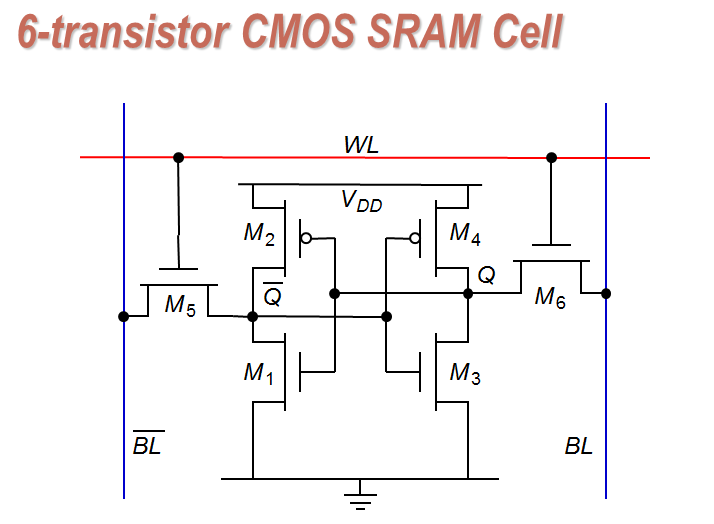
555 timer:

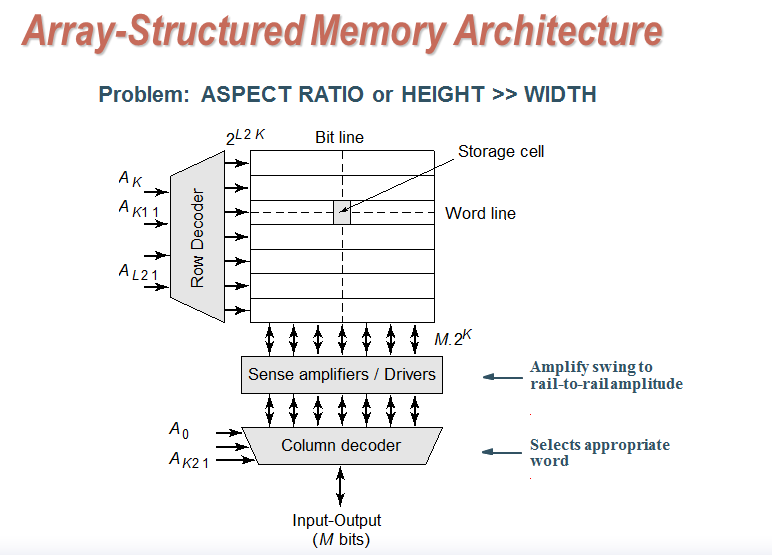


Astable (square wave) Monostable (Single pulse of fixed width)

Memory:



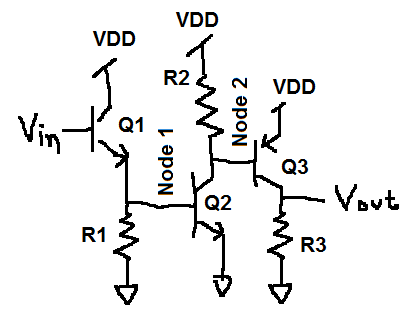




Exam:

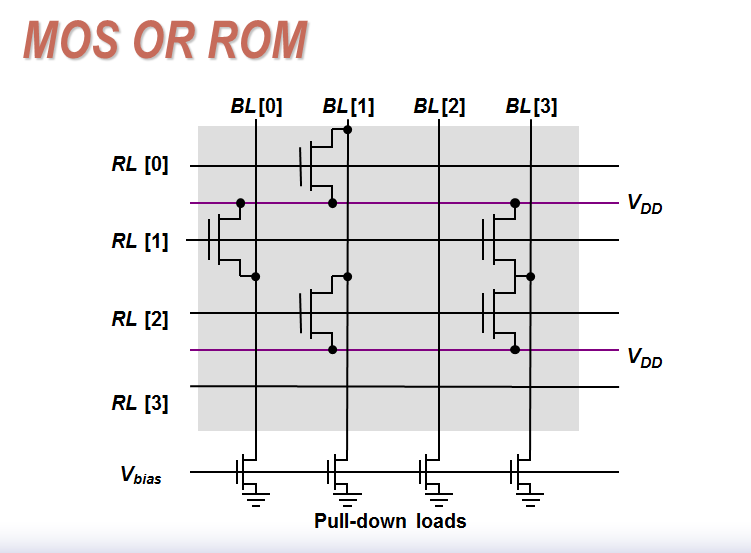
1. Regions of operation. Questions 1a through question 1c assume: VT=0.65V, VBE**ON**=0.3V, VBC**ON**=0.45V, and VCESAT=0.2V. (Total: 6 pts – 3pts each)
   1. Draw a pnp. Draw in voltages at the terminals that would put the pnp in the linear region.
   2. Draw a NMOS. Draw in voltages at the terminals that would put the NMOS in the active region.
2. Propagation delays and energy (Total: 13 pts – 3pts, 5pts, 5pts)
   1. How much energy is used for the tpHL transition?
   2. Set up the general equation for how much **energy** is used for a Low to High transition to where Vout=for a circuit that has an R and C of R and C.
   3. Set up the general equation for the **delay** of a Low to High transition to where Vout=for a circuit that has an R and C of R and C.
3. In Circuit 1, (Total: 9 pts – 3pts each)
   1. where might you see the Miller capacitance? In other words, between which nodes? Or in other words, which capacitance will be affected?
   2. what is the value of that perceived capacitance? (The Miller capacitance)
   3. what is the total capacitance you see at Node 1 in CIRCUIT 1. Answer in terms of CGD, CDB, CBE or whatever Capacitance names are needed.

**CIRCUIT 1:**



1. Short answer questions: (Total: 22 pts – 2pts each)
   1. What are the three types of power dissipation you see in a CMOS circuit?
   2. Explain each type of power dissipation.
   3. What’s the difference between a dynamic and a static circuit?
   4. What is ratioed logic?
   5. What’s the difference between ROM and RAM?
   6. What’s the difference between a stack and RAM or ROM?
   7. Why would you use DRAM instead of SRAM?
   8. What is the cost (drawback) of using DRAM over SRAM?
   9. Why are sense amplifiers used in memory?
   10. What are the definitions of trise, tfall, tpHL, and tpLH?
   11. In CIRUIT 2, if I set RL(2) to ‘1’ and RL(0)=RL(1)=RL(3)=’0’, what would I see on BL(3), BL(2), BL(1) and BL(0)?

**CIRCUIT 2:**



1. Draw a DCVSL circuit that implements . If you don’t remember DCVSL, half credit for drawing a pseudo NMOS circuit. (Total: 6 pts)
2. Draw the VTC for a Schmitt trigger that looks like (and is) a CMOS inverter. VDD = 1V, VTP=0.7V, VTN=0.6V. Draw marks on X-axis and Y-axis. (Total: 5 pts)
3. Setup and hold time violations. Note that the output of FF1 is also an input to the delay. (Total: 10 pts. 5pts each) **CIRCUIT 3:**

FF0

D0 Q0

Clock

FF1

D1 Q1

Delay

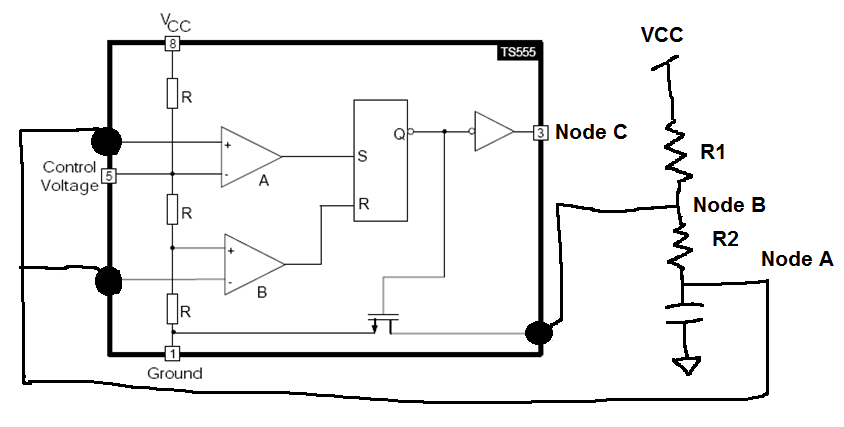
3ns < Delay < 5ns

|  |  |  |
| --- | --- | --- |
|  | Flip flop 0 | Flip Flop 1 |
| Hold time | 6ns | 6ns |
| Setup time | 10ns | 20ns |
| TclkQ | 5ns ≤ TclkQ ≤ 9ns | 2ns ≤ TclkQ ≤ 11ns |

* 1. Ignoring hold time violations, what is the shortest period that will allow this circuit to run without setup time violations? Show all work. You may use math or a timing diagram but you don’t need to show both. One or the other.
  2. How many paths give hold time violations? Show the math.

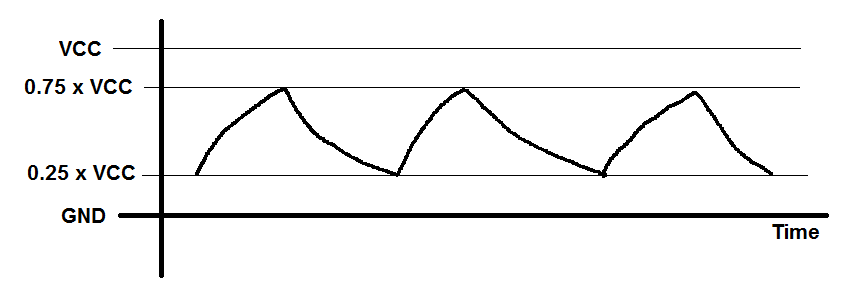
1. 555 timer: (Total: 8 pts. 4 pts each)

**Circuit 4:**



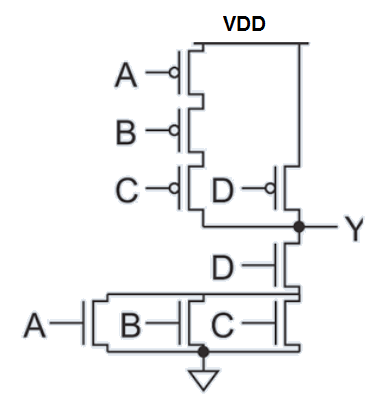
* 1. If you built the 555 timer in Circuit 4 from discrete parts and you could change any of the Rs and Cs, what would you change to get the following signal at Node A to look like:

**GRAPH 1:**

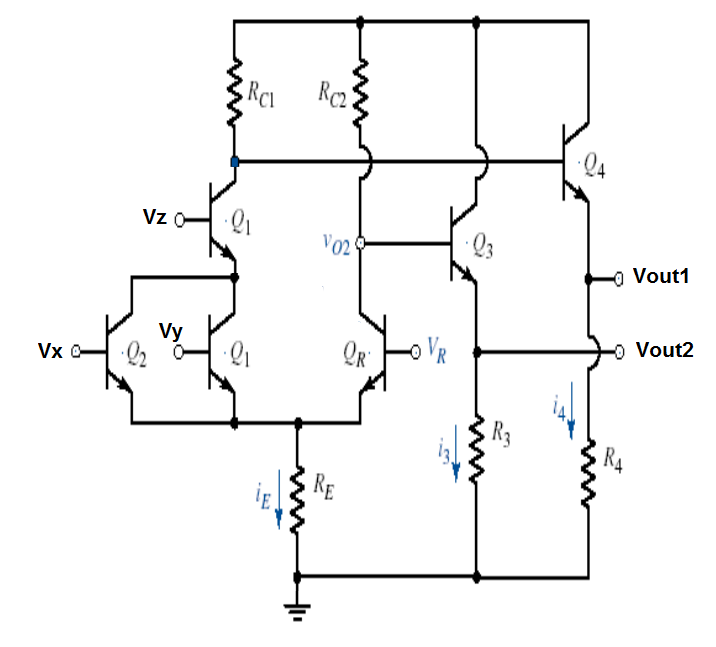


* 1. Draw the voltage at Node C for Graph 1. Draw it on Graph 1 so I can see the relationship between the voltage at Node A and Node C.

1. For each of the following circuits, tell me what their logic function is, what the logic family is, and what Vout maximum and minimum are. The logic function should look something like:  and the Vout maximum and minimum should be generalized like: VoutMAX=VDD-VTN. Write the logic equation as close to the actual circuit as you can. Don’t DeMorgan-ize it to make it prettier or anything like that. If the voltage is determined by a particular current, make sure to use that current in your equations. (Total: 10pts. 5 pts each)
   1. CIRCUIT 5:



* 1. CIRCUIT 6:



1. Vout: (Total: 7pts. 5 pts, 2pts)
   1. Draw a load line sketch (don’t do math – just approximate) for a RTL inverter. Draw in two load lines on the graph. One line is for a BIG resistor and the other load line for a small resistor.
   2. How does Vout change when R gets bigger?